

BOOK PROSPECTUS

Power Integrity for Nanoscale Integrated Systems

A practical handbook for designing with power supply noise

Authors

Masanori Hashimoto & Raj Nair

Contact information

Email: hasimoto@ist.osaka-u.ac.jp, raj@anasim.com

Anasim Corp.

3838 E Encinas Ave, Gilbert, AZ 85234
USA

TITLE

Power Integrity for Nanoscale Integrated Systems

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BRIEF DESCRIPTION

Power Integrity (PI), as it relates to everyday life, is the stability and robustness of the electrical power supply to homes and businesses. For example, how stable is the 115V AC supply voltage level? How stable is its frequency (60 cycles a second) that determines time accuracy in simple electrical clock mechanisms? How steady is this supply when an air-conditioner system's large compressor kicks on and pulls substantial current and power from this supply? Do the lights dim when one turns on a food grinder/mixer in the kitchen? Does the transient disturbance in the supply 'reset' any electronic device?

Very similar concerns apply to highly integrated electronic systems as well, such as those in the nanoscale fabrication regimes. Most integrated circuit (IC, chip) supplies are "DC", or constant-potential difference supplies. Here, concerns relate to how constant this potential difference remains within the chip, how does the difference diminish or expand based upon sections of an integrated circuit turning on and off, the power spectral content of such variations etc. Static and dynamic changes in this power supply potential difference impact integrated circuit performance in detrimental ways, therefore necessitating accurate evaluation of such changes for any IC design and their impact upon overall chip performance.

As chips continue to scale according to [Moore's Law](#) (which predicted that the number of transistors per unit area of a chip doubles approximately every 18 months), and progress to holistic integration (sometimes referred to as "More-than-Moore" [a catch phrase for everything from [exaggerated integration ambitions](#) to [advertisement for a FAB](#)] or the non-traditional integration of dissimilar technologies and diverse functionalities on a single chip), PI challenges continue to increase at an alarming rate. For example, *where transistors double in a digital chip area, noise doubles too...* but this has remained largely unnoticed by the electronic design automation industry. This is of concern particularly because

chip and system power consumption has shown an alarming and unexpected trend of increasing, rather than decreasing, as technology scales. Additionally, operating frequencies are increasing steadily, leading to sharper digital signal transitions and therefore higher frequency content in supply currents that amplifies inductive noise. Inductive noise is harder to compute and therefore to predict, is susceptible to long-range interactions between wires, and leads to electromagnetic interference with sensitive circuits. Nanoscale chips, therefore, face a [Power Integrity Wall](#). This aspect is only now being comprehended in the industry.

Our first book in this subject matter, "[Power Integrity Analysis and Management for Integrated Circuits](#)", discussed implications to power integrity (PI) due to semiconductor scaling in detail. It was revealed that despite containment of chip power consumption, the PI challenge continues to increase exponentially, necessitating both advanced analysis methods and management solutions. This is borne out by actual examples from the industry in 2010, for example, a performance issue (inability to attain desired operating frequency without errors) on a chip at a large integrated device manufacturer, where two relatively high-power cores interacted with one another on a chip power grid. Tests on first silicon revealed that the chip operating voltage needed to be raised by as much as 7%, defeating the low-power nature of the component. State-of-the-art industry tools failed to detect a problem prior to the chip being fabricated, and continued to fail in debugging the problem post-silicon. As predicted, PI is of greater concern at lower operating voltages of nanoscale chips.

We believe what is equally important is comprehensive understanding of the impact of power integrity degradation upon all aspects of nanoscale integrated circuit design. At lower operating voltages, and consequently reduced "noise margins" or tolerance of errors, electronic circuits are increasingly susceptible to noise in their power supplies. Traditional characterization of circuits, employing analog circuit design methods, calculated a value of "power supply rejection ratio" or PSRR to denote a measure of supply noise tolerance of circuits. PSRR is computed and plotted in the frequency domain, while most circuit functionality and performance within chips is verified in the time domain, with circuit PSRR not readily correlated with circuit performance. Digital circuits also do not define a PSRR, but employ "noise margin" as a measure of circuit robustness. Rigorous understanding of circuit tolerance or susceptibility to various aspects of PI degradation is hence not readily available in the literature.

For instance, a question that has remained unanswered in CMOS digital design is the following. What is of greater importance for voltage droop: the depth or amplitude of the droop (reduction in available supply differential), or its width, which is the duration for which the power supply droops? Designers often employ gross approximations, such as maximum droop amplitude, or a value called full-width-half-max (FWHM) to characterize voltage droop and its potential impact. FWHM represents droop as a step reduction in power supply of one-half the voltage droop amplitude for the entire duration of droop occurrence. What is not clear, put succinctly, is how PI degradation is to be represented in a manner similar to signal-to-noise ratio (SNR) as is done for information signals, and the connection between such a measure of power supply quality and circuit robustness. There is hence a substantial lack of rigor in understanding such aspects of power supply degradation and circuit tolerance. This understanding is particularly important for nanoscale design given exponentially increasing PI degradation as revealed in [1].

It is this need, and attention to circuits not included in the prior publication, that we aim to fulfill in this second book as a natural continuation. While [1] reveals and teaches about PI, its exponential relation to semiconductor scaling, analysis techniques, and methods of management, this effort focuses upon circuit architecture and design, and practical knowledge in designing circuits and systems with PI degradation in view.

Approach

This book is intended to be a continuing rigorous treatment of an area of VLSI design that is seeing a thirst equivalent to that seen for Signal Integrity a decade and a half ago. We intend to explore, in a most comprehensive manner, all aspects of power integrity impact upon integrated circuit architecture and design, from theoretical and practical standpoints, and help readers appreciate the significance of power integrity to nanoscale integrated electronics design. For example, our recent article on [PI and IC Floorplanning](#) points out the significance of PI awareness in a connection between PI and Thermal aspects in IC design and 3D integration of nanoscale chips. Power consumption is directly related to heat generation, since as much energy is spent in charge transfer pathways as is stored in capacitance, and the spent energy dissipates as heat. Hot spots for power consumption in an integrated circuit are also locations requiring advanced power management techniques such as power gating; this results in associated PI issues. Investigating PI with accurate tools, therefore, provides an early indication of potential

thermal issues in the chip. We show that one can rapidly simulate a “physical design” of an integrated circuit, and not just its circuit design, deriving information helpful to the optimization of on-chip and on-package resources. Solutions for PI degradation mitigation, such as additional via's and metal also help with heat conduction out of the chip, thus serving a valuable dual purpose.

Beginning with clear proof, both theoretical and empirical, of how power integrity manifests as a critical issue in nanoscale chips, we intend to dispel many of the myths (page 16) prevalent in the industry relating to PI. We will then proceed to explore the impact of PI upon important classes of circuits, such as analog, digital, and mixed-signal circuits. Discussing the impact of supply and substrate noise in these circuit types, we will explore architectural, circuit, and process techniques that render these circuits more robust in the presence of anticipated PI degradation. We also intend to compare pre-nanoscale (square-law MOSFET) and nanoscale integrated circuits to determine the trend for circuit robustness with changing transistor characteristics. Specific systems within an integrated circuit, such as Clock Generation and Clock Distribution, have particular sensitivity to PI degradation; we explore design of such systems to minimize impact, while also minimizing PI degradation caused by these systems. Input-Output (IO) circuits, similarly, have specific sensitivity to supply noise and we intend to discuss various signaling techniques advancing data throughput and signal-to-noise ratio in the presence of significant supply noise. Taking a specific signaling technique that is intended to be sensitive to supply noise, we intend to explore “link budgeting”, which partitions available signal timing and amplitude between communications link elements for a given transfer rate. Link budget and SNR are impacted very significantly by supply noise as discussed briefly in [1], Chapter 5, and we intend to explore robust link budgeting and design in the presence of significant PI degradation.

We also intend to discuss modeling of various circuits and high-level functional blocks (or cores) for accurate, true-physical PI analysis. We believe that as integration includes the third dimension in the nanoscale fabrication regime, high levels of abstraction with physics-based simulations form the solution to accurate and early analysis of PI degradation, permitting front-end resource optimization and low cost/low energy designs. With hands-on examples, we intend to show how such abstraction and modeling of circuits and cores facilitates optimal IC physical design. We aim to explore modeling of PI degradation as well, resolving differences between PSRR, Noise Power, FWHM representations and the like, and explore the capture of PI degradation in a

general metric such as SNR for signals, or as specific metrics depending upon the class of circuits considered. A gap between board-level frequency domain power delivery network impedance characterization and spatio-temporal chip-level time domain simulations remains to be bridged, and we intend to explore this aspect as part of our work.

With the exponential increase in PI degradation with scaling as the challenge studied, we intend to discuss state-of-the-art industrial developments and solutions in integrated circuit design and fabrication that address PI and on-chip signaling issues. For example, clock gating, power gating, and dynamic voltage and frequency scaling, all techniques for low power and energy consumption, impact on-chip PI, and will be discussed. Augmenting a discussion on the relationship of noise to jitter, we intend to discuss the impact of noise on digital logic timing in further detail. Operating temperature is of increasing concern in nanoscale systems due to its exponential impact on leakage, and we intend to explore PI implications and system design addressing this aspect. In addition to the continuation of increased metal layers and capacitance in chips and 3D systems, we will explore the challenges and opportunities presented by several technological advances in the nanoscale era. 3D ICs utilizing Through-Silicon-Vias (TSV's) - vertical interconnects very different from traditional vias - have enabled circuit integration in the third dimension. We will analyse the significant role played by TSV's in managing PI challenges, for example power distribution and heat dissipation in multiple active layers. Moreover, recent years have brought significant progress in developing carbon-based interconnects with carbon-nanotubes (CNT's) or graphene nanoribbons (GNR's). These nano-materials have remarkable electrical and thermal conductivity properties. For the first time, this book will address the implications of this nascent technology from a power supply management perspective.

OUTSTANDING FEATURES

- Our book will be the first in the industry that will focus upon the impact of power integrity degradation upon various analog, digital, and mixed-signal circuits in nanoscale fabrication regimes.

- Dispelling myths in the industry, such as “My design is low power, it has no power integrity issues”, “My design is low frequency, I do not have any di/dt problems”, “My chip/package interface has very low inductance – why will I have PI issues”, we will explore the close relationship between PI and SI (signal integrity) and reveal a looming challenge with SI given exponential PI degradation with scaling.
- The book will be the first to explore modeling of circuits for advanced PI analysis and modeling of PI degradation that relates closely to circuit and system performance akin to SNR for signals. Our treatment of PI as a design parameter and variable will be a first.
- The book will explore the impact of PI degradation on circuits and systems of critical importance to nanoscale chips, such as clock generation, distribution, and IO sub-systems, with specific examples, and illustrate instances of circuit-PI co-design.
- It will provide hands-on training in, and demystify, advanced power integrity analysis for circuits, systems such as communications links, and chips, facilitating optimal nanoscale integrated circuit design.

PROBLEMS SOLVED

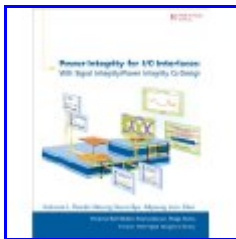
This book will fill a critical GAP in nanoscale integrated electronics design and verification. In continuation of work captured in [1], which revealed exponentially growing PI degradation with scaling from fundamentals, this book will reveal circuits and systems susceptibility and robustness with PI degradation. Demystifying advanced PI analysis for circuits and systems, it will attempt to bridge the gap between the current frequency-domain-centric board-level PI analysis methods with spatio-temporal awareness in time-domain analysis at the chip level. Focusing on “holistic integration”, the book will be the first to address technology advancements in nanoscale semiconductor fabrication addressing the exponentially growing problem of power integrity degradation. Combined with [1], this book will provide ample material for a new course in VLSI design and engineering addressing power integrity, energy, and design.

READER BENEFITS

Readers will be introduced to rigorous theoretical clarification and detailed treatment of power integrity susceptibility and robustness for nanoscale circuits and systems absent in any current text. They will benefit from decades of power delivery, integrity analysis and management

experience and innovation of the authors as well as work conducted in the research divisions of companies such as Intel. They will learn the close relationship between PI and SI for key circuits and systems in chips. They will work with hands-on examples of robust circuit design with PI in view, as well as advanced power integrity analysis on circuits and chips. They will also learn with specific design examples optimal chip floorplanning and design minimizing PI degradation, PI-related circuit performance degradation, and chip power/energy consumption. In continuing learning from [1], students and other academic readers will find the circuits and systems focus of this work complementing the first book very well, enhancing the potential for a PI course in electrical engineering curriculum.

COMPETITION



[Power Integrity for I/O Interfaces: With Signal Integrity/ Power Integrity Co-Design \(Prentice Hall Modern Semiconductor Design Series\)](#) by [Vishram S. Pandit](#), Woong Hwan Ryu, and Myoung Joon Choi (Hardcover - Oct 22, 2010)

Signal and power integrity in digital systems: TTL, CMOS, and BiCMOS

[James E. Buchanan](#) Westinghouse Electric Corp., Baltimore, MD

Pandit et al's book above approaches closest to being competition to the effort we contemplate. Pandit restricts his work to a discussion of I/O interfaces and SI/PI co-design w.r.t. I/O interfaces, which is one aspect of one class of circuits that may be integrated. Pandit's book, while discussing a significant aspect of integrated circuit and system design, and its challenges with PI degradation, does not address PI impact upon circuits in general, and provides an overview of existing system- or board-level methods, techniques and prior art, such as SSO/SSN or simultaneous switching outputs and simultaneous switching noise, supply noise, ground bounce, etc., which therefore do not have to be dealt with in very much detail in our work. Pandit's book does not address the

nanoscale challenges for PI, nor does it foresee or discuss rise in PI degradation and its corresponding SI impact. This book also appears to focus excessively on aspects of signal integrity and its discussion, which detracts from a comprehensive discussion of power integrity. Rather than being true competition, Pandit's book provides a supporting treatment of current IO interface implementations such as DDR, and associated PI concerns, while our effort discusses PI-sensitive true-differential links, that are generally accepted as the future of high-speed interfaces, in one chapter, and devotes other chapters to discussions of many other circuit classes essential to integrated circuit design.

A substantial portion of our book will be based on detailed academic research and experimental findings in the field of integrated circuit power integrity. It is intended to be a text supporting an engineering course on VLSI design with emphasis upon power, power integrity, and energy consumption management. Our book will also include findings emanating from research into circuits and PI at the research labs of Intel corporation that arguably led the industry in semiconductor and electronic system scaling. While we intend to discuss signal integrity degradation as one of the consequences of PI degradation, this will not be the primary focus of our work as it is in works that may be considered to be competition. Continuity of fundamental learning offered by the prior publication [1] also differentiates our work from others in this field.

APPARATUS

All traditional techniques for learning will be included, such as questions, problems, case-studies, project reports, reference papers, patents, glossaries etc. Additionally, we intend to provide continuing learning to readers through our company website (www.anasim.com, pioneering PI analysis and PI-aware chip design) which will offer readers access to the latest research work in this arena, as also to web-logs or BLOGs that will help them through interactive learning and collaboration opportunities.

Computer simulation exercises may be carried out with SPICE, with some exercises done through PI-FP available through Anasim at minimal expense for educational purposes. Anasim is working

with major EDA tool vendors to integrate power-integrity-aware front-end IC design capabilities in current tool suites made available in most educational institutions.

TARGET AUDIENCE

This book is intended for students, researchers, system designers, and engineers in nanoscale electronics design. It is intended to bringing about in-depth understanding of custom circuit design addressing a critical and minimally addressed aspect of nanoscale ULSI, which is power integrity and its impact upon circuits, chips, and 3D assemblies of electronic components.

It will be written at the 'Senior' level extending into 'Graduate' study and research, permitting students to absorb fundamentals as well as proven circuit modeling and design techniques enabling efficiency in nanoscale design. It is intended to be part of a main or elective course for students in the completion of their undergraduate education in electrical engineering, specifically, VLSI design, while offering them the opportunity for advanced learning and research in graduate study. The case-studies and examples within will additionally serve as references to practicing engineers and chip architects, who are also expected to benefit from discussions of power integrity impact to circuits previously available only to those in the industry specializing in such work. Prerequisites for students will include engineering mathematics, physics, computer programming and reasonable knowledge of electronic system and VLSI circuits/chip design.

The combination of Analog, Digital, and IO circuits and systems, addressing a state-of-the-art design aspect, will make the book indispensable to practicing electrical and communications / computer engineers as well as those specializing in ULSI design. With the industry heading relentlessly toward miniaturization and portability, and enhanced automation of all functions such as locomotion, food, and medicine, advanced electronics integration, energy efficiency, and deep-nanoscale design are critical industry requirements. This book, that addresses PI, a key aspect enabling this industry direction, will be a “must-have” for all practicing engineers in the field. An introduction to advanced technologies solving the exponential problem of PI will also provide a comprehensive treatment of the subject matter.

Market Considerations

In 2008, the number of [electrical, electronics and computer engineers](#) amounted to approximately 375,000 in the United States. Another [survey](#) indicates that computer engineers (of which VLSI design is a specialization) hold approximately 79,000 jobs of the roughly one and a half million engineering jobs in the US, growing at an estimated 4% rate. Japan, UK, Europe, and Australia also form a substantial market for advanced VLSI engineering texts with comparable growth. The vast majority of growth in VLSI design engineering jobs is in Asia, with India and China being the most vibrant markets. In all, the global total available market for advanced VLSI engineering texts may be approximately 20,000, with a growth of about 5%, or 1000 per annum. A greater market is in academic institutions globally, with the number of reputable engineering colleges exceeding 500 in India alone. Assuming a count of 1000 institutions teaching VLSI design globally, and approximately 10 VLSI graduates on average, penetration into the engineering curriculum, through comprehensive coverage in [1] and this work, can multiply annual book sale count to 5000 or more, an order of magnitude greater than average expectations for an engineering book. At a book price of say €100 (100 Euro), **annual revenues** from book sales can be **0.5 million Euro at the high end**.

We are in preliminary discussions with universities around the globe to teach a course in low energy design and PI. The lead author of this effort is an associate professor at one of the top universities in Japan. We believe that as nanoscale electronic design becomes mainstream, PI will be an essential component of VLSI design in the electrical and electronics engineering curricula.

Organizations such as the IEEE, its Circuits and Systems society, and the CPMT will be appropriate professional networks for marketing. Conferences such as the ISSCC, DAC, ISCAS, ISLPED, etc. and related trade shows for nanoscale design will also be good venues for book publicity. The book is a must-read for anyone facing nanoscale IC optimization, low-energy and power integrity management challenges.

Example Figures

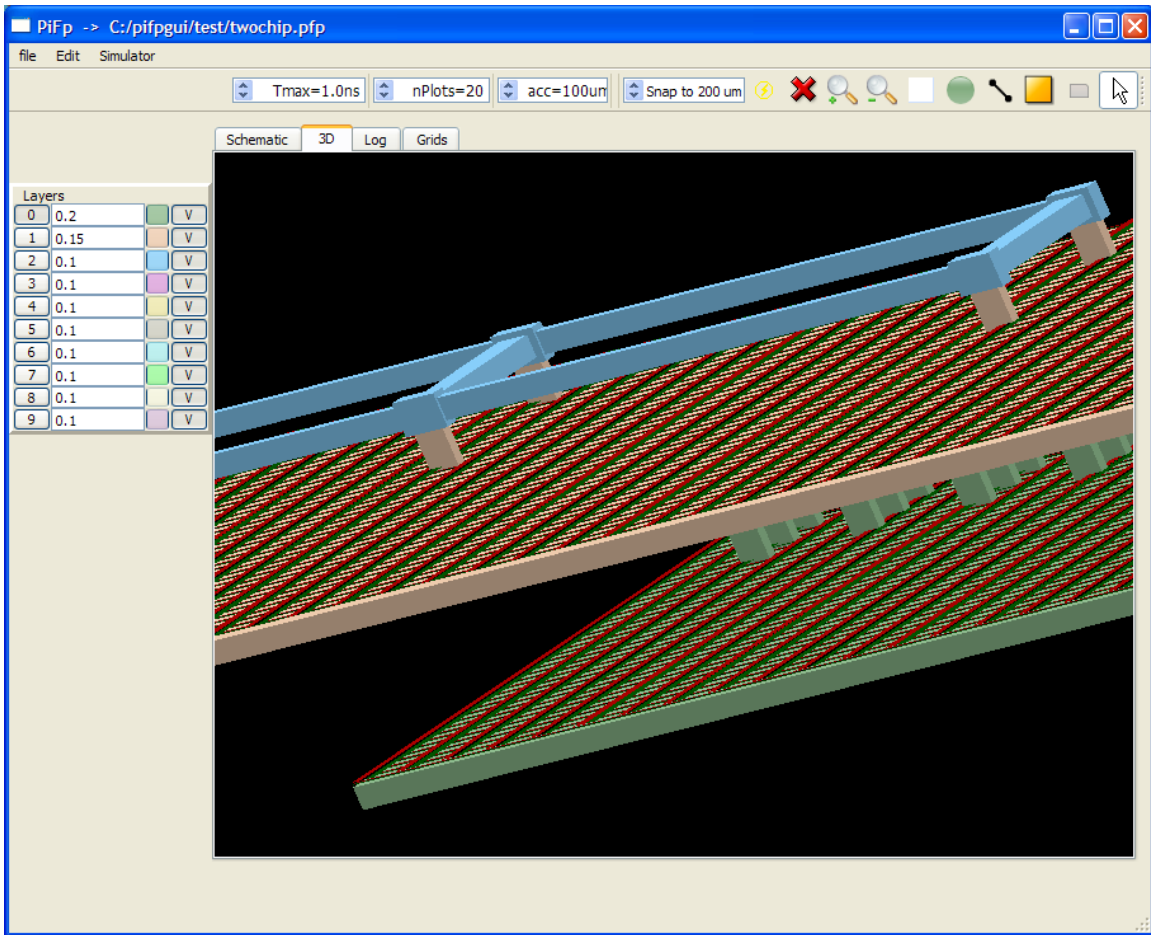


Figure 1: IC physical design schematic capture for advanced PI analysis

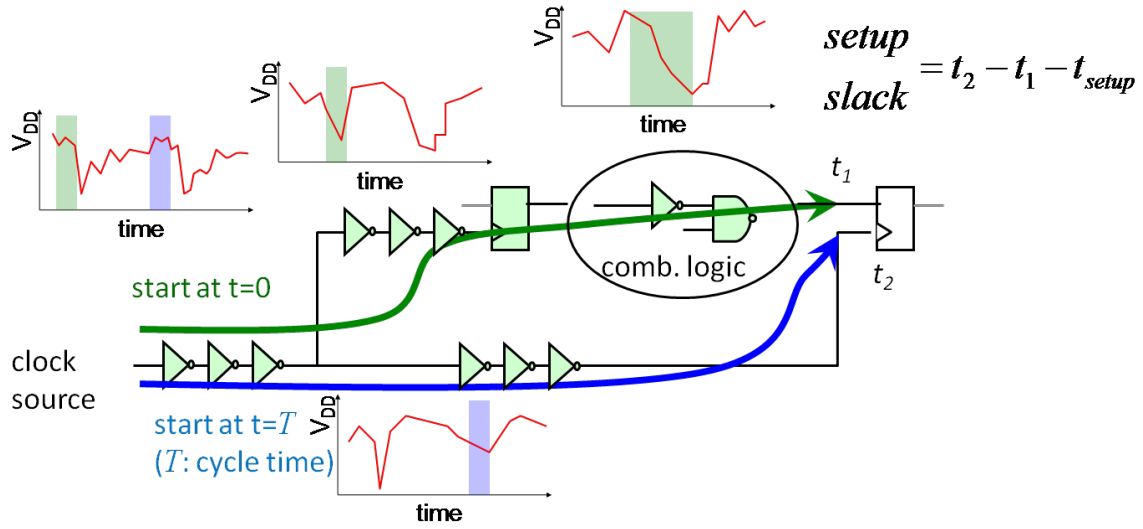


Figure 2: Impact of power supply noise on timing

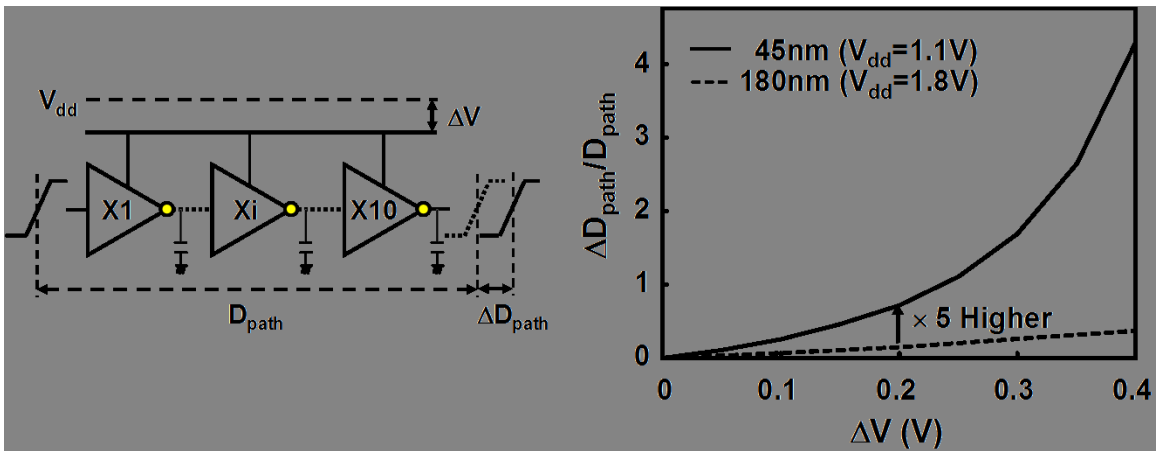


Figure 3: Sensitivity of Gate Delay on Voltage

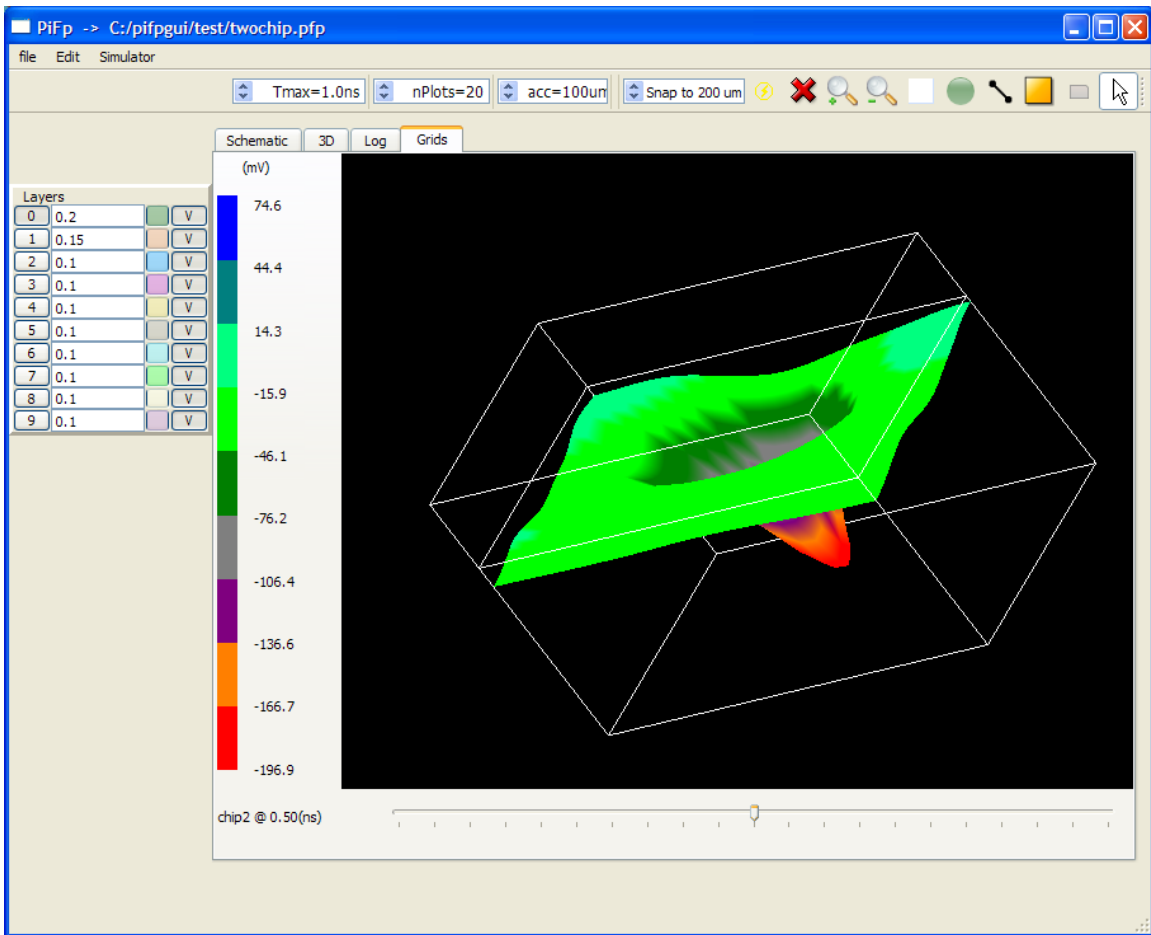


Figure 4: Example simulation result for PI on a layer of a 3D chip stack

Status / Authors

Articles and papers published to date can contribute a significant amount of material to the book. The authors believe that with concerted effort, most of the book's material can be compiled by the October 2012.

Brief Author Biographies



Masanori Hashimoto, Ph.D., is an associate professor in the department of information systems and engineering, Osaka university. He has been working for modeling and measurement of on-chip power supply noise and signal coupling noise. His research interests also include timing analysis, ultra low power design, design for reliability and on-chip high-speed signaling. He received Ph.D. degree from Kyoto university in 2001. His CV is found at <http://www-ise2.ist.osaka-u.ac.jp/~hasimoto/index.html.en>



Raj Nair, M.S. is an expert consultant in IC power delivery and power integrity, and co-founder of [Anasim Corp.](#) developing and marketing [TI-fp](#). Prior to Anasim, he founded ComLSI, Inc. that developed and licensed patents and silicon IP in advanced power delivery as well as high-speed signaling. Formerly, he was with Intel Corp., where he conceived and implemented distributed on-chip voltage regulation in microcontrollers and championed a fully integrated CMOS voltage regulator microprocessor power delivery solution. He holds **40+ issued patents, 1 book**, and numerous online, conference, and journal publications. His detailed biography may be viewed at ComLSI or Anasim websites. His CV is at this [link](#).

Draft Chapters Outline

1. SIGNIFICANCE OF POWER INTEGRITY FOR INTEGRATED CIRCUITS

Introduce the impact of power integrity on circuits and systems in general. Dispel myths: “My design is low power, it has no power integrity issues”, “My design is low frequency, I do not have any di/dt problems”, “My design has very low inductance – why will I have PI issues?”, “Scaling increases on-die capacitance in each process generation, and with power remaining the same, I won't have any problems with power integrity!” Cite actual industry examples where PI issues resulted in chip rework (recent Texas Instruments problem with an advanced SoC, containing an ARM core + DSP core on a power supply causing speed problems, requiring increase in supply voltage by ~7%), discuss energy consumption/low power challenges. Introduce low power techniques and PI impact of Clock Gating, Power Gating, and DVFS. Briefly introduce the relationship between PI and SI: PI degradation leading to significant SI issues, such as timing errors, jitter, glitches and incorrect data etc. Discuss the concept of PSRR, for digital and analog circuits, and introduce the reader to challenges (if any) to power supply rejection ratio for circuits in the nanoscale regimes. Briefly review causes of PI degradation, challenges with scaling, the spatio-temporal nature of PI within chips etc. from our previous book. Discuss limitations with prior analysis techniques and potential benefits of new methods.

2. SUPPLY AND SUBSTRATE NOISE IMPACT ON CIRCUITS

Discuss supply and substrate noise (for common nanoscale fabrication processes, bulk, SOI etc.) and their impact on digital, analog, and mixed-signal circuits. Discuss “single-ended noise”, PWR noise, GND noise, and “differential noise” or “supply compression” and impact. Common logic families and noise margin analysis. Analog (amplifiers, bandgap voltage references) and mixed-signal circuits (A2D, D2A) and performance degradation. Digital (flip flops, logic families and gates) and dynamic (domino etc.) circuits and digital timing performance impact. Discuss circuits co-design with PI if applicable: Stanford noise feedback into a voltage regulator for critical noise-sensitive circuits, for example. Discuss examples, solutions and experimental results.

3. CLOCK GENERATION AND CLOCK DISTRIBUTION WITH PI DEGRADATION

PLL's specifically, and supply and substrate noise induced performance degradation. Explore concepts to minimize PLL performance degradation due to noise induced by digital circuits within the PLL. Clock distribution topologies (CTS, custom designs including grids, tiles, bars etc.) and impact of supply variation/noise on skew/jitter. Discuss Clocking and PI co-design. Discuss the importance of including inductance in clock distribution analysis (Intel Labs research work on a [GHz router chip](#)). Discuss low-jitter clock buffer design (research at Intel labs, US patent, etc.). Explore differential clocking and clock distribution, and resonant/standing-wave clocking (US patent). Review non-clocked (asynchronous) designs and explore PI degradation impact in the nanoscale (leakage dominated) regime. Discuss solutions and experimental results.

4. CHIP IO CIRCUITS AND PI

Discuss on and off-chip signaling trends, and low-power design constraints. Touch upon SSO and SSN, briefly discussing IO and PI co-design. Compare single-ended signaling with differential signaling. Analyze and compare a “true differential” ([CBDS](#)) signaling driver's output signal degradation and a “quasi differential” signaling driver's output SNR impact due to supply noise. Review link budgeting for a communications system, and discuss the impact of PI degradation on link amplitude/timing budgeting and bit error rate (BER). Compare, if possible, PAM/QAM methods of signaling with raw binary signaling for throughput and robustness with PI degradation. Discuss examples, solutions, and experimental results.

5. MODELING OF CIRCUITS AND IP CORES FOR PI ANALYSIS

Review modeling techniques – SPICE, simplifications, macro/behavioral models, IBIS etc., and continuum modeling. Discuss PI analysis using vectored and vector-less simulations. Discuss power delivery network modeling in RC and RLC form, and challenges with on-chip inductance inclusion. Discuss EDA tools status, particularly relating to inductance inclusion (Navin Srivastava's method integrated into Calibre and others). Discuss modeling and analysis challenges with 3D integration. Can one really simulate a physical design for electrical aspects? Illustrate the use of high levels of abstraction and physics-based, non-SPICE simulations for true-electromagnetic analysis (employing [pi-fp](#)). Provide analysis examples and discuss benefits.

6. POWER INTEGRITY DEGRADATION AND MODELING

Review PSRR for analog and digital circuits. Discuss types of PI degradation. Discuss FD and TD aspects of PI degradation. Discuss power supply noise spectrum, static and dynamic noise, FWHM etc., and explore a Power-to-Noise ratio metric in the frequency domain and the time domain for PI degradation with static and dynamic voltage variations in the supply differential. Discuss limitations of such a metric because of the spatial (locational) and temporal (phase) dimensions of PI degradation. Determine if performance of a majority of nanoscale circuits correlates with any chosen PNR metric. Modeling of effects closely related to PI, such as thermal effects / determination of front-end thermal operating conditions for circuits to narrow range of thermal verification.

7. LOW POWER TECHNIQUES AND PI IMPACT

Discuss common techniques for low power: Clock Gating, Power Gating, Dynamic Voltage and Frequency scaling. Show PI impact of each of these techniques on a typical chip. Discuss techniques for mitigation of PI impact of such techniques. Discuss block and chip design enhancements to ensure robustness in a degraded supply environment.

8. CHIP TEMPERATURE AND PI IMPACT,

Discuss relationship between chip temperature and leakage/PI. Discuss the potential for thermal exaggeration of PI degradation (IR Drop). Detail an early thermal analysis flow and chip interconnect/3D stack optimization for temperature. Discuss design enhancements to ensure robustness in a high temperature and degraded supply environment.

9. CASE STUDY: CHIP ZZZZZ, INFERENCES AND CONCLUSIONS

Study an SoC chip design in a nanoscale process in simulations and silicon (if possible). Discuss design enhancements to ensure robustness in a degraded supply environment. Review inferences and conclusions from all chapters and case studies discussed in the book. Review trends and solutions for the future.

10. PI IN THE NANOTECHNOLOGY REALM

Review traditional advances in number of metal layers, thick top metal layers, package assistance to and enhancement of chip PI, MIM or other integrated capacitance etc. Is a sea-change in interconnect necessary to address PI (and SI)? Or will computational circuits change inherently with technologies such as [PMC](#), or the [MEMRISTOR](#), once again changing electrical aspects such as PI, and resource needs such as metal and charge/energy storage? Review non-traditional advances in IC back-end fabrication technology. Discuss 3D IC challenges such as limited interface connections to outside world and heat dissipation. Describe through-silicon vias (TSVs) and their role in mitigating these challenges. Present fundamental properties of carbon nano-materials - carbon nanotubes (CNTs) and graphene nanoribbons (GNRs). Discuss state-of-the-art for their integration into CMOS process. Discuss fabrication challenges for nano-materials with respect to power integrity/power distribution needs. Discuss PI specific implications of using carbon nano-material based global distribution layers and TSVs based on electrical and thermal modeling.

Other details

Estimated number of pages:	500
Illustrations:	100+
Other contributors to the book (as of Prospectus writing):	3 contributors
Book chapters compiled in (with PDF copies):	OpenOffice Writer
Illustrations:	Digital / Hand drawn

Online articles relating to Power Integrity from the authors (data on 09/23/10)

EntryID	Views	Item, (Date Entered), Category
24772	7273	Power Integrity and Energy-Aware Floorplanning (1/16/2008) SOCcentral Contributed Article
25302	6494	A Power Integrity Wall Follows the Power Wall! (3/25/2008) SOCcentral Contributed Article
25778	1620	Beyond IR Drop: Dynamic Voltage Droops and Total Power Integrity (5/22/2008) SOCcentral Contributed Article
31446	1425	Continuum (Analog) Analysis of Power Integrity (5/28/2010) SOCcentral Contributed Article
31901	445	IC Floorplanning and Power Integrity (8/2/2010) SOCcentral Contributed Article

Sales of the first PI book focused on IC's

“PI Analysis and Management for Integrated Circuits” sold ~**300** books in 2010 from its release date of May 7, 2010. Sales results for the second half of 2010 are anticipated by April 1, 2011.

References

- [1] [Power Integrity Analysis and Management for Integrated Circuits, ISBN 0137011229, Nair & Bennett, May 2010](#)
- [2] On the applicability of single-walled carbon nanotubes as VLSI interconnects, Navin Srivastava et al, IEEE Transactions on Nanotechnology, Vol. 8, No. 4, July 2009
- [3] Published papers and articles relating to topics in draft chapters outline.